

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L7	139	simulat\$4 and (double adj buffer) and race	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/05/27 16:54
L9	13	simulat\$4 and (fifo same race)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/05/27 17:07
L10	115	simulat\$4 and (queue same race)	US-PGPUB; USPAT; EPO; DERWENT	OR	ON	2007/05/27 17:07


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fifo race

1950

- 2004

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[Race Analysis of Traces of Asynchronous Message-Passing Programs - all 5 versions »](#)

KC Tai - Proc. of the 17th International Conference on Distributed ..., 1997 - doi.ieeecs.org
 ... 3.2 **Race** analysis of SR-sequences of type **FIFO** ... 2 shows an SR-sequence of type **FIFO** and the **race** set for each receive in this SR-sequence. ...

Cited by 16 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

[Race-free interconnection networks and multiprocessor consistency - all 6 versions »](#)

A Landin, E Hagersten, S Haridi - Proceedings of the 18th annual international symposium on ..., 1991 - portal.acm.org

Page 1. **Race-free** Interconnection Networks and ... Thus the access graph must be acyclic, and sequen- tial consistency is guaranteed 3 **Race-free** networks n T lw-rj ...

Cited by 32 - [Related Articles](#) - [Web Search](#)

[RASSP Technology Insertion Into the Synthetic Aperture Radar Image Processor Application - all 3 versions »](#)

J Pridgen, R Jaffe, W Kline - Proceedings of 2nd Annual RASSP Conference, Arlington, VA, 1995 - atl.lmco.com

... the signal pro- cessors. The 4k-deep output **FIFO** provides data buffering between the **RACE** interface and the Hot Rod transmit port. ...

Cited by 5 - [Related Articles](#) - [View as HTML](#) - [Web Search](#)

[How to solve the Santa Claus problem - all 6 versions »](#)

M Ben-Ari - Concurrency - Practice and Experience, 1998 - doi.wiley.com

... there are no condition variables. Also note that since Java queues are not **FIFO**, **race** conditions are possible. RELATED WORK ON JAVA ...

Cited by 8 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

[Optimizing a FIFO, scalable spin lock using consistent memory - all 7 versions »](#)

I Rhee - Real-Time Systems Symposium, 1996., 17th IEEE, 1996 - ieeexplore.ieee.org

... paper, we improve on Craig's work present- ing a **FIFO**, scalable spin ... The FSSL al- gorithm uses memory consistency to solve potential data-**race** problems among ...

Cited by 2 - [Related Articles](#) - [Web Search](#)

[\[CITATION\] A cell based MAC protocol with traffic shaping and a global FIFO strategy](#)

C Blondia, O Casals, J Garcia - **RACE** Open Workshop Broadband Access, Nijmegen, The ..., 1993

Cited by 1 - [Related Articles](#) - [Web Search](#)

[FIFO queued entry point circuit for a network interface card - all 3 versions »](#)

BB Lo, K Uppunda, AL Pan - US Patent 6,360,278, 2002 - Google Patents

... packets with the network because memory pointers can be directly pushed onto the transmit **FIFO** by the processor without encountering **race** conditions. ...

Cited by 3 - [Related Articles](#) - [Web Search](#)


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fifo race simulation

1950

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All Results[L Pantel](#)[J Rohlf](#)[P Levis](#)[L Rizzo](#)[L Wolf](#)**On the impact of delay on real-time multiplayer games**

L Pantel, LC Wolf - Proceedings of the 12th international workshop on Network ..., 2002 - portal.acm.org

... This RC-Car **simulator** has been developed by one of the authors ... scheme has been implemented in the 'Virtual RC **Racing**' game using a **FIFO** buffer where ...[Cited by 93](#) - [Related Articles](#) - [Web Search](#)**RASSP Technology Insertion Into the Synthetic Aperture Radar Image Processor Application - all 3 versions »**

J Pridgen, R Jaffe, W Kline - Proceedings of 2nd Annual RASSP Conference, Arlington, VA, 1995 - atl.lmco.com

... By using the same function specifications as the CP_Callable library for the application the CP pro- gram could be verified by **simulation**. ... **FIR FIFO RACE PORT** ...[Cited by 5](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)**A Memory Efficient Architecture for Real-Time Parallel and Perspective Direct Volume Rendering - all 4 versions »**

H Ray, D Silver - Rutgers Univ., New Brunswick, NJ, Tech. Rep. CAIP-TR-237, 1999 - caip.rutgers.edu

... **Simulation** results are presented in the next section. ... In its current implementation, **RACE** has four volume memory modules, pixel memory modules, and ... Ray **FIFO** ...[Cited by 10](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)**Multi-player entertainment system - all 3 versions »**

RS Jacobs, GB Isdale, WM Porada - US Patent 6,126,548, 2000 - Google Patents

... as **race** cars or aircraft, have become extremely popular. The popularity of the games has led to the development of increasingly sophisticated **simulation** systems ...[Cited by 8](#) - [Related Articles](#) - [Web Search](#)**SYNCHRONIZATION AND BLENDING OF PLURAL IMAGES INTO A SEAMLESS COMBINED IMAGE - all 2 versions »**

RS JACOBS, JL DAVIS, WM PORADA, DS SAMSON - 2003 - freepatentsonline.com

... The particular approach includes a first-in-first-out (**FIFO**) technique that recognizes when the ... In the case of a **race** car, the **simulator** station preferably ...[Cached](#) - [Web Search](#)**IRIS performer: a high performance multiprocessing toolkit for real-time 3D graphics - all 7 versions »**

J Rohlf, J Helman - Proceedings of the 21st annual conference on Computer ..., 1994 - portal.acm.org

... A pfDisplList may be configured as a **FIFO** or ring buffer for concurrent producer/consumer configurations. ... The **racing** car **simulator** shown in Figure 15 uses ...[Cited by 275](#) - [Related Articles](#) - [Web Search](#)**TOSSIM: accurate and scalable simulation of entire tinyOS applications - all 37 versions »**

P Levis, N Lee, M Welsh, D Culler - Proceedings of the first international conference on ...,


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fifo asynchronous race simulation

1950

- 2004

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All Results[K Yun](#)[K Stevens](#)[P Beerel](#)[A McAuley](#)[S Rotem](#)
[Delay models for verifying speed-dependent **asynchronous** circuits - all 2 versions »](#)

 JR Burch - Computer Design: VLSI in Computers and Processors, 1992. ..., 1992 - [ieeexplore.ieee.org](#)

 ... them in the verification of a **FIFO** controller circuit ... used for verifying speed-dependent **asynchronous** cir- cuits ... When doing **simulation**, it might not be necessary ...

[Cited by 13](#) - [Related Articles](#) - [Web Search](#)
[ASIM-An **asynchronous** architectural level simulator - all 2 versions »](#)

 D Nellans, VK Kadaru, E Brunvand - Proceedings of GLSVLSI, 2004 - [cs.utah.edu](#)

 ... level, and **asynchronous** systems at any level, is a major ad ... correct startup of threads to avoid **race** conditions due ... data items to be in flight in **FIFO** order on ...

[Cited by 1](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#)
[... -wave combined approach with runtime reconfiguration for designing a low latency **asynchronous** FIFO](#)

 JG Lee, SJ Kim, JA Lee, E Kim, K Kim - Advanced System Integrated Circuits 2004. Proceedings of ..., 2004 - [ieeexplore.ieee.org](#)

 ... **Race** and Metastability Issues The signaling rules of ... Since the proposed **FIFO** is working

 elas- tically ... However, the **asynchronous** and concurrent tran- sitions of ...

[Cited by 1](#) - [Related Articles](#) - [Web Search](#)
[Dynamic **asynchronous** logic for high-speed CMOS systems - all 6 versions »](#)

 AJ McAuley - Solid-State Circuits, IEEE Journal of, 1992 - [ieeexplore.ieee.org](#)

 ... requires careful and computation- ally intensive **simulation** because the ... Phase alignment

 is inherently **asynchronous**. Unlike the guaranteed **race**- and hazard-free ...

[Cited by 11](#) - [Related Articles](#) - [Web Search](#)
[Design of **asynchronous** circuit primitives using MOS current-mode logic \(MCML\)](#)

 TW Kwan, M Shams - Microelectronics, 2004. ICM 2004 Proceedings. The 16th ..., 2004 - [ieeexplore.ieee.org](#)

 ... This **race** condition results in longer response time and ... 'The double-edge-triggered fligflop is the storage element in our **asynchronous** MCML **FIFO**. ...

[Web Search](#)
[\[BOOK\] Testing **Asynchronous** Circuits: A Survey - all 5 versions »](#)

 H Hulgaard, SM Burns, G Borriello - 1994 - [cs.washington.edu](#)

 ... Some delay assumptions must be made in order to construct useful **asynchronous** circuits. ...

 The **FIFO** element in Figure 5 [41] is an example of a speed-independent ...

[Cited by 54](#) - [Related Articles](#) - [View as HTML](#) - [Web Search](#) - [Library Search](#)
[Synthesis of self-timed **FIFO** circuit from signal transition graphs \(STGs\)](#)


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fif asynchronous race

1950

- 2004

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All Results[K Yun](#)[K Stevens](#)[P Beerel](#)[K Tai](#)[S Rotem](#)

Race Analysis of Traces of Asynchronous Message-Passing Programs - all 5 versions »

KC Tai - Proc. of the 17 thInternational Conference on Distributed ..., 1997 - doi.ieeecs.org

... In this paper we have shown a definition of a message **race** and three **race** analysis algorithms for programs using **asynchronous** communication, **FIFO** ordering and ...

Cited by 16 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Delay models for verifying speed-dependent asynchronous circuits - all 2 versions »

JR Burch - Computer Design: VLSI in Computers and Processors, 1992. ..., 1992 - ieeexplore.ieee.org

... We describe the verification of a speed- dependent, **asynchronous FIFO** controller circuit that demonstrates that the binary inertial delay model can be ...

Cited by 13 - [Related Articles](#) - [Web Search](#)

Dynamic asynchronous logic for high-speed CMOS systems - all 6 versions »

AJ McAuley - Solid-State Circuits, IEEE Journal of, 1992 - ieeexplore.ieee.org

... is easier-but combining dynamic and **asynchronous** logic is more difficult. We must guarantee mini- mum refresh intervals, together with **race**- and hazard-free op ...

Cited by 11 - [Related Articles](#) - [Web Search](#)

... between multiple non-synchronous systems utilizing an asynchronous FIFO that uses asynchronous ... - all 3 versions »

SR Masteller... - US Patent 6,308,229, 2001 - Google Patents

... Assistant Examiner—Abdelmoniem Elamin (74) Attorney, Agent, or Firm—Steptoe & Johnson

LLP (57) ABSTRACT An **asynchronous FIFO** using **Asynchronous NULL** Con ...

Cited by 5 - [Related Articles](#) - [Web Search](#)

RAPPID: An asynchronous instruction length decoder - all 19 versions »

S Rotem, K Stevens, R Ginosar, P Beerel, C Myers, ... - ... on Advanced Research in **Asynchronous** Circuits and Systems, 1999 - doi.ieeecomputersociety.org

... The **FIFO** is **asynchronous**, but its implementation details are not described here, as it is used only as an interface to the tester. ...

Cited by 50 - [Related Articles](#) - [Web Search](#)

... -wave combined approach with runtime reconfiguration for designing a low latency asynchronous FIFO

JG Lee, SJ Kim, JA Lee, E Kim, K Kim - Advanced System Integrated Circuits 2004. Proceedings of ..., 2004 - ieeexplore.ieee.org

... **Race** and Metastability Issues The signaling rules of ... Since the proposed **FIFO** is working

elas- tically ... However, the **asynchronous** and concurrent tran- sitions of ...

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FIFO using asynchronous logic to interface between clocked logic circuits -


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All Results

[C Li](#)
[R Kao](#)
[W Browder](#)
[J Vitter](#)
[A Aravin](#)

Double buffering operations between the memory bus and the expansion bus of a computer system - all 7 versions »

PR Culley, M Taylor - US Patent 5,519,839, 1996 - Google Patents

... Kimball & Krieger [57] ABSTRACT **Double buffering** operations to ... A system data **buffer**

coupled between the main ... the expansion bus includes 256-bit **double** read and ...

Cited by 26 - [Related Articles](#) - [Web Search](#)

Early activation of transcription factor NF-κB during ischemia in perfused rat heart - all 3 versions »

C Li, W Browder, RL Kao - American Journal of Physiology- Heart and Circulatory ..., 1999 - Am Physiological Soc

... Chuanfu Li, William Browder, and **Race L. Kao** ... 3, 14) in a 15-μl binding reaction mixture containing 1× binding **buffer** [50 μg/ml of **double**-stranded poly(dI-dC ...

Cited by 107 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Method and apparatus for dynamic chaining of DMA operations without incurring race conditions - all 3 versions »

M Sodos... - US Patent 5,367,639, 1994 - Google Patents

... **Doublebuffer**-ing is performed in the following manner. ... in CCBi 220 the first channel control block **buffer**. ... CCBs without incurring errors due to **race** conditions ...

Cited by 23 - [Related Articles](#) - [Web Search](#)

Early activation of IKKβ during in vivo myocardial ischemia - all 3 versions »

C Li, RL Kao, T Ha, J Kelley, IW Browder, DL ... - American Journal of Physiology- Heart and Circulatory ..., 2001 - Am Physiological Soc

... Chuanfu Li 1, **Race L. Kao** 1, Tuanzhu Ha 1, Jim Kelley 2 ... in 15 μl of binding reaction mixture containing 1× binding **buffer** [50 μg/ml **double**-stranded poly ...

Cited by 24 - [Related Articles](#) - [Web Search](#) - [BL Direct](#)

Method and apparatus for the prevention of race conditions during dynamic chaining operations - all 3 versions »

M Sodos... - US Patent 5,251,312, 1993 - Google Patents

... formed. **Double buffering** is performed in the following ... block **buffer**. The chip control status bit 240 would ... While the controller logic 230 is S **race** conditions. ...

Cited by 28 - [Related Articles](#) - [Web Search](#)

Double buffering technique for binocular imaging in a window - all 14 versions »

JS McVeigh, VS Grinberg, MW Siegel - Stereoscopic Displays and Applications VI, Proceedings of ..., 1994 - cs.cmu.edu

... com- mand to avoid a **race**-condition; if ... In the discussion of **double buffering** the original purpose ... The **double buffer** alleviates the dependence on processor and ...

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Double-stranded RNAs in mitochondrial extracts of stem rusts and leaf rusts of cereals - all 2 versions »


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IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

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2001 Page(s):1 - 1690
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31 January 1994 Page(s):1
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Stevens, K.; Ginosar, R.; Rotem, S.;
Advanced Research in Asynchronous Circuits and Systems, 1999. Proceedings., Fifth Internationa
19-21 April 1999 Page(s):208 - 218
Digital Object Identifier 10.1109/ASYNC.1999.761535
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Abstract Full Text: PDF(1565 KB) IEEE STD |
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2001 Page(s):1 - 310
Abstract Full Text: PDF(1664 KB) IEEE STD |
| <input type="checkbox"/> | 7. Dynamic asynchronous logic for high-speed CMOS systems
McAuley, A.J.;
Solid-State Circuits, IEEE Journal of
Volume 27, Issue 3, March 1992 Page(s):382 - 388
Digital Object Identifier 10.1109/4.121561
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IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

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 Dongai Dai; Panda, D.K.;
Computers, IEEE Transactions on
 Volume 48, Issue 2, Feb. 1999 Page(s):236 - 244
 Digital Object Identifier 10.1109/12.752665
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- ☐ 2. Dynamic asynchronous logic for high-speed CMOS systems
 McAuley, A.J.;
Solid-State Circuits, IEEE Journal of
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- ☐ 3. Flow enforcement algorithms for ATM networks
 Dittmann, L.; Jacobsen, S.B.; Moth, K.;
Selected Areas in Communications, IEEE Journal on
 Volume 9, Issue 3, April 1991 Page(s):343 - 350
 Digital Object Identifier 10.1109/49.76632
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Solid-State Circuits, IEEE Journal of
 Volume 37, Issue 12, Dec. 2002 Page(s):1901 - 1927
 Digital Object Identifier 10.1109/JSSC.2002.1088121
[AbstractPlus](#) | Full Text: [PDF\(364 KB\)](#) IEEE JNL
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- ☐ 5. An asynchronous, high-speed packet switching component
 Budde, W.O.; Keller, H.-G.; Reuerman, H.-J.; van de Wiel, P.;
Design & Test of Computers, IEEE
 Volume 11, Issue 2, Summer 1994 Page(s):33 - 42
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 Digital Object Identifier 10.1109/12.752665
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 Jagd, A.; Myken, S.; Phillips, C.; Theologou, O.; Giamniadakis, J.; Migliarina, G.;
[Broadband Services, Systems and Networks, 1993., Second International Conference on](#)
 3-4 Nov 1993 Page(s):65 - 69
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 2001 Page(s):i - 1690
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 Stevens, K.; Ginosar, R.; Rotem, S.;
[Advanced Research in Asynchronous Circuits and Systems, 1999. Proceedings., Fifth International](#)
 19-21 April 1999 Page(s):208 - 218
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 Gibbs, S.; Arapis, C.; Breiteneder, C.; Lalioti, V.; Mostafawy, S.; Speier, J.;
 Multimedia, IEEE
 Volume 5, Issue 1, Jan.-March 1998 Page(s):18 - 35
 Digital Object Identifier 10.1109/93.664740
 AbstractPlus References Full Text: PDF(1276 KB) IEEE JNL
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 Randall, M.;
 Micro, IEEE
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 House, R.;
 Spectrum, IEEE
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 Scott, M.L.;
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| <input type="checkbox"/> | <p>5. A 32-bit VLSI digital signal processor
 Hayes, W.P.; Kershaw, R.N.; Bays, L.E.; Boddie, J.R.; Fields, E.M.; Freyman, R.L.; Garen, C.J.; Hs
 J.J.; Miller, C.R.; Mondal, K.; Moscovitz, H.S.; Rotblum, Y.; Stocker, W.A.; Tow, J.; Tran, L.V.;
 Solid-State Circuits, IEEE Journal of
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IEEE STD	IEEE Standard

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 Randall, M.;
[Micro, IEEE](#)
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